A Transmit/Receive IF Chip Set for WCDMA Mobiles in 0.35-μm CMOS

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***Abstract*—An implementation of the IF section of WCDMA mobile transceivers with a set of two chips fabricated in an inexpensive 0.35-μm two-poly three-metal CMOS process is presented. The transmit/receive chip set integrates quadrature modulators and demodulators, wide dynamic range automatic gain control (AGC) amplifiers, with linear-in-decibel gain control, and associated circuitry. This paper describes the problems encountered and the solutions envisaged to meet stringent specifications, with process and temperature variations, thus overcoming the limitations of CMOS devices, while operating at frequencies in the range of 100 MHz–1 GHz. Detailed measurement results corroborating successful application of the new techniques are reported. A receive AGC dynamic range of 73 dB with linearity error of less than $\pm$2 dB and spread of less than 5 dB for a temperature range of $-30\,^{\circ}$C to $+85\,^{\circ}$C in the gain control characteristic has been measured. The modulator measurement shows a carrier suppression of 35 dB and sideband/third harmonic suppression of over 46 dB. The core die area of each chip is 1.5 mm^2.**

***Index Terms*—CMOS analog integrated circuits, code division multiaccess, gain control, IF systems, transceivers.**

I. Introduction

PRECISION differential analog circuits in IF circuits of WCDMA transceivers operating in the 100-MHz–1-GHz frequency range have traditionally been implemented using bipolar devices [1]–[5] because of their superiority in terms of matching, noise, transconductance, gain-bandwidth, and repeatability over their CMOS counterparts. Some reported CMOS implementations, however, rely on an enhanced digital content to overcome the shortcomings of the devices [6]. However, such an approach requires high-speed analog-to-digital converters (ADCs) that are difficult to design.

Thanks to the continued downscaling of process technology, CMOS devices now exhibit adequate high-frequency performance (f_T around 30 GHz for a 0.35-μm N-channel device) to be used in such applications. However, such performance is obtained only if short channel and, in some cases, minimum-channel-length devices are used. Obviously, this gives rise to increased transistor mismatches resulting in poor differential performance and offset voltages. The performance of high-frequency precision differential CMOS analog circuits, therefore, suffers heavily due to this problem.

Looking at another aspect, high precision and stability of performance have mainly been obtained in low-frequency circuits by application of negative feedback, trading off voltage gain. However, for such high-frequency circuits, negative feedback is often difficult to apply because of stability problems. To maintain stability in such cases, the gain bandwidth of an amplifier usually has to be reduced. On the other hand, use of an open-loop amplifier structure with a small amount of local feedback may be feasible in such cases, but the consequent changes in performance parameters with process and temperature will have to be compensated for.

Overcoming the above-mentioned problems with innovative circuit techniques, we have achieved a high level of performance coupled with the highest integration level known to us for WCDMA IF transmit/receive chip sets in CMOS technology using a 0.35-μm two-poly three-metal process. The transmit-chip integrates an automatic gain control (AGC) amplifier, a quadrature modulator (up-converter), and a buffer for driving 50-Ω off-chip load. The AGC circuit involves new techniques to realize a precise linear-in-decibel gain control characteristic. This characteristic is further compensated against temperature and process variations using a new gain compensating bias generator. The novel inductorless 50-Ω buffer features unity gain, which is difficult to achieve since CMOS source followers are known to exhibit huge signal losses because of inadequate transconductance. The receive-chip integrates another AGC amplifier and a quadrature demodulator (down-converter). Both chips are equipped with quadrature local oscillator (LO) generators while operating from a single power supply of 3.0 V$\pm$10% for an ambient operating temperature of $-30\,^{\circ}$C to $+85\,^{\circ}$C. The demodulator and LO amplifiers also use a new approach—capacitively source coupled differential stages—to suppress dc offsets. The chips have a core die size of 1.5 mm^2 each.

II. Circuit Description

A. Chip Architecture

Fig. 1 shows the block diagram of the system. The transmit signal path contains the in-phase quadrature (I/Q) modulator, a 25-dB attenuator, and an AGC amplifier. A quadrature LO generator generates $f_{\rm LO}$–I and $f_{\rm LO}$–Q at 380 MHz for the modulator from a 760-MHz reference source $f_{\rm REF}$. The receive signal

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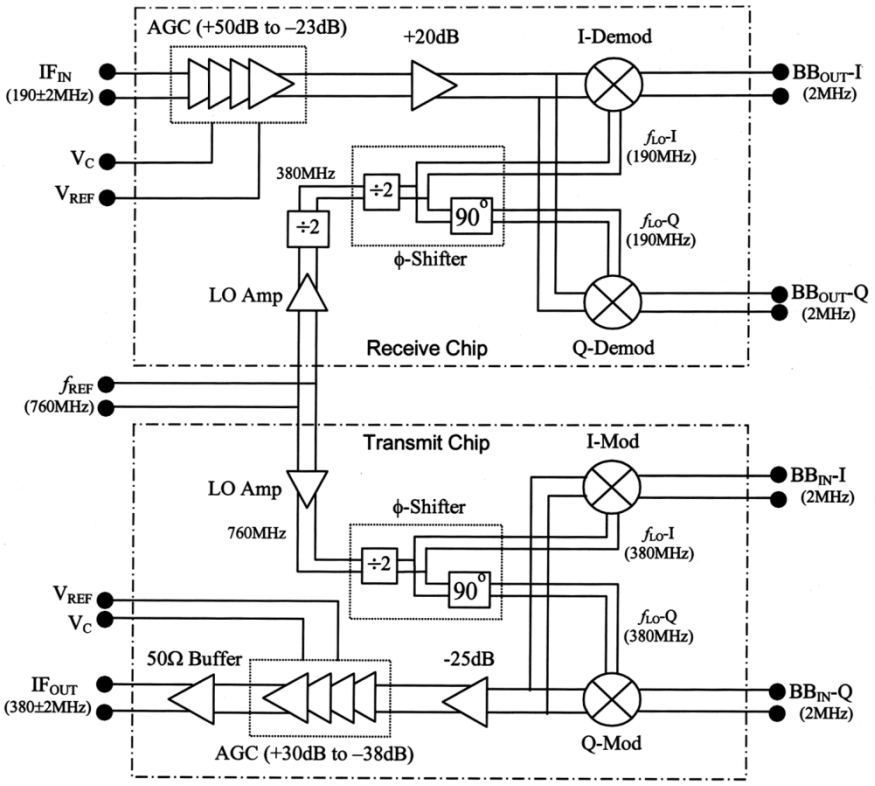

Fig. 1. Block diagram of WCDMA transmit/receive chip set.

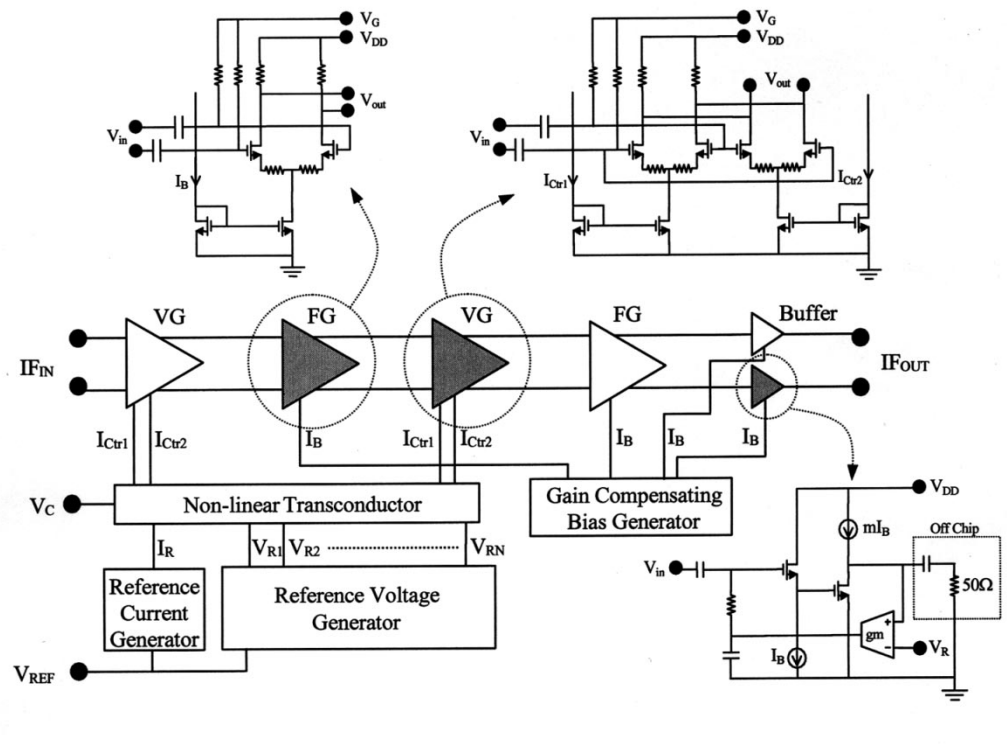

Fig. 2. Amplifiers and 50-Ω buffer for AGC section.

path begins with another AGC amplifier followed by a 20-dB gain amplifier and an I/Q demodulator. Another LO generator derives the required quadrature signals at 190 MHz for the demodulator from the same 760-MHz reference frequency.

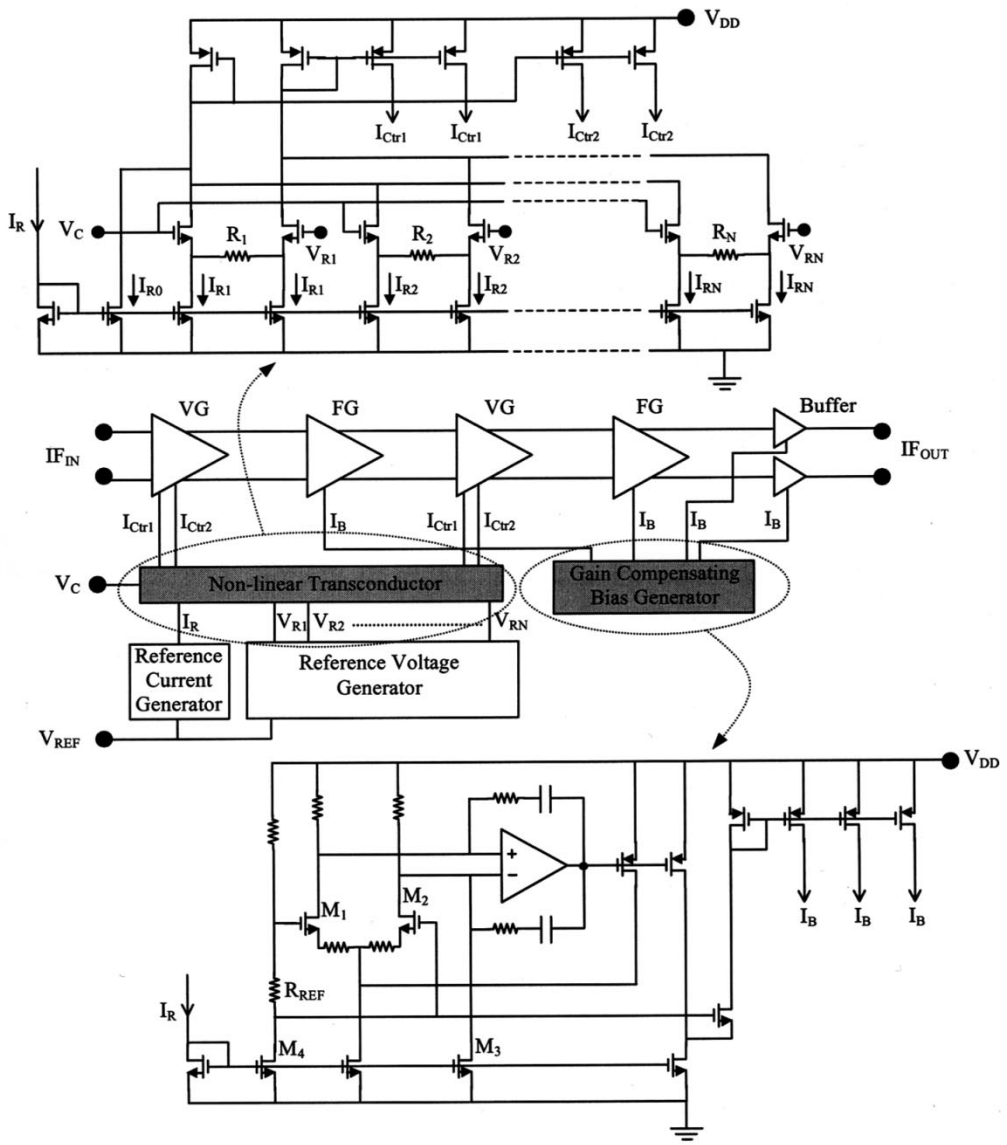

Fig. 3. Gain control and compensation circuitry for an AGC section.

B. Transmit and Receive AGC Amplifiers

The AGC amplifiers in the transmit and receive chips are designed to have a dynamic range (gain control range) of approximately 70 dB. The operating frequencies of these amplifiers are 380 MHz (transmit IF frequency) ± 2 MHz (message sidebands) and 190 MHz (receive IF frequency) ± 2 MHz (message sidebands) with maximum gains of $+30$ and $+50$ dB, respectively. The gain of each amplifier is controlled by an external dc voltage V_C varying from 0.4 to 2.4 V with a linear-in-decibel characteristic. The frequency response of each amplifier needs to be flat within ± 0.25 dB throughout the operating frequency range.

Fig. 2 shows the common architecture used for both transmit and receive AGC amplifiers. It is organized as a cascade of fixed gain (FG) and variable gain (VG) stages for a good compromise between signal-to-noise ratio and signal-handling capabilities. The VG and FG stages are designed to have frequency responses in the range of 600–900 MHz so that the overall frequency response requirements are met. To meet such frequency requirements, differential devices of 0.35-μm (minimum feature size of the technology) channel length had to be used. Since minimum channel devices cannot be matched well, both the FG and VG stages employ coupling capacitors at the inputs to prevent propagation and amplification of the offset voltages. The stages also use source degeneration resistors for better linearity and lower offset voltages. The VG stages are based on the Gilbert cell topology and the gain is varied by adjusting the difference of the bias currents I_{Ctr1} and I_{Ctr2}. Such topology allows a very wide dynamic range—around 35 dB per stage—to be realized.

C. 50-Ω Buffer

This buffer is used at the output of the transmit AGC amplifier only, to drive a 50-Ω external resistive load. The traditional source-follower buffer is extremely difficult to design for 0-dB voltage gain, but for this application, such a require-

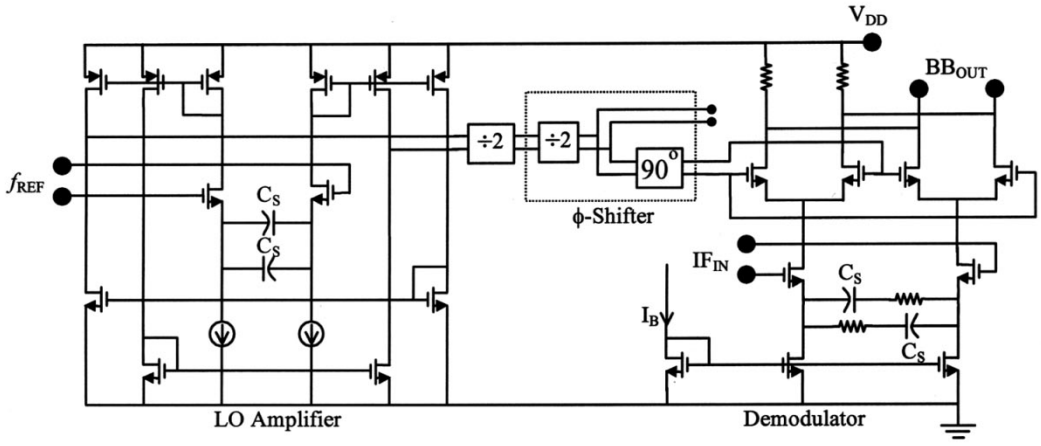

Fig. 4. LO amplifier and demodulator circuits.

ment is essential to keep the number of stages in the amplifying chain as low as possible to maintain the frequency response. The problem mentioned is better perceived from the expression of voltage gain A_v (neglecting body effect) for the source follower as given by

$$A_v = \frac{g_m R_L}{1 + g_m R_L} \tag{1}$$

where g_m is the transconductance of the source-follower transistor and R_L is the load resistance that it drives. It can be seen from (1) that the relationship $g_m \gg 1/R_L$ needs to be satisfied to obtain 0-dB voltage gain, which, in turn, leads to the fact that the g_m of the source follower needs to be at least 200 mS while driving a 50-Ω load.

Keeping this difficulty in mind, a new buffer with 0-dB voltage gain has been conceived and is shown in Fig. 2. It basically consists of a combination of a source-follower and a common-source amplifier (using minimum-channel-length transistors), the former being used to buffer the input capacitance of the latter. The external load resistance is capacitively coupled to the drain of the output transistor. The dc operating point of the output transistor is fixed with a current source through its drain and an active feedback from that point via a single low-frequency pole g_m-C filter, as shown. The g_m-C filter allows only low-frequency feedback to take place, thereby allowing full signal amplification through the forward path. If the transconductance of the output stage is chosen appropriately, the voltage gain of the new buffer at signal frequencies is given by

$$A_v = g_m R_L = 1. \tag{2}$$

It is easy to see that, in this case, the g_m of the output transistor is required to be no more than 20 mS while driving a 50-Ω load.

D. Nonlinear Transconductor

The circuit details of the nonlinear transconductor are shown in Fig. 3. This block generates pairs of currents I_{Ctr1} and I_{Ctr2} for controlling the gains of the VG stages in response to the control voltage V_C. Since the gain has to be varied linearly in decibel values, a suitable nonlinear transconductance is required, which will also compensate for the bias current-to-gain relationship of the MOS amplifiers. For this purpose, I_{Ctr1} and I_{Ctr2} are obtained by summing up currents from several differential voltage-to-current (*V/I*) converters. These *V/I* converters operate linearly in small staggered ranges (approximately given by $2I_{\mathrm{RI}} \cdot R_I$, $I = 1 - N$) centred around reference voltages V_{RI} spanning the entire range of V_C. The *V/I* converters have different transconductances given by $1/R_I$. The reference voltages V_{RI} are obtained from a single temperature-independent reference voltage V_R. Similarly, the reference currents I_{R0}, I_{RI} are derived from a single nearly temperature-independent current reference I_R, which, in turn, is obtained from V_R and an internal resistor. When I_{RI} and R_I are chosen appropriately with some overlap between the ranges, a smooth transfer characteristic with the desired nonlinearity can be obtained. Since the differential transistors in VG stages are of minimum channel length, the gain variation of such stages with bias current cannot

TABLE I
SUMMARY OF MEASURED RESULTS/PARAMETERS FOR WCDMA IF CHIP SET

Parameter	Transmit-chip	Receive-chip	Units
LO/IF frequency f_{LO}	380.0	190.0	MHz
Channel/message bandwidth	5.0/2.0	5.0/2.0	MHz
Reference frequency f_{REF}	760.0	760.0	MHz
AGC control voltage V_C	0.4-2.4	0.4-2.4	V
Maximum gain @ V_C=2.4V	–5.0	70.0	dB
Minimum gain @ V_C=0.4V	–73.0	–3.0	dB
Dynamic range	68.0	73.0	dB
Linearity error	±2.0	±2.0	dB
Noise Figure (R_S=1K)		6.4	dB
Input P1dB (at max. gain)	1.5	–67.35	dBm
LO suppression	35.0		dBc
Sideband suppression	46.0		dBc
3rd harmonic suppression	47.0		dBc
O/P noise floor (at max. gain)	-123.0		dBm/Hz
ACPR at P_{OUT} = –10dBm	-51.0		dBc
I/Q amplitude mismatch		< 1.0	dB
I/Q phase error		±2.0	degrees
Supply voltage V_{DD}	3.0±10%	3.0±10%	V
Supply current – active	31.0	17.0	mA
Supply current – standby	<10.0	<10.0	μA
Core die area	1.5	1.5	mm^2

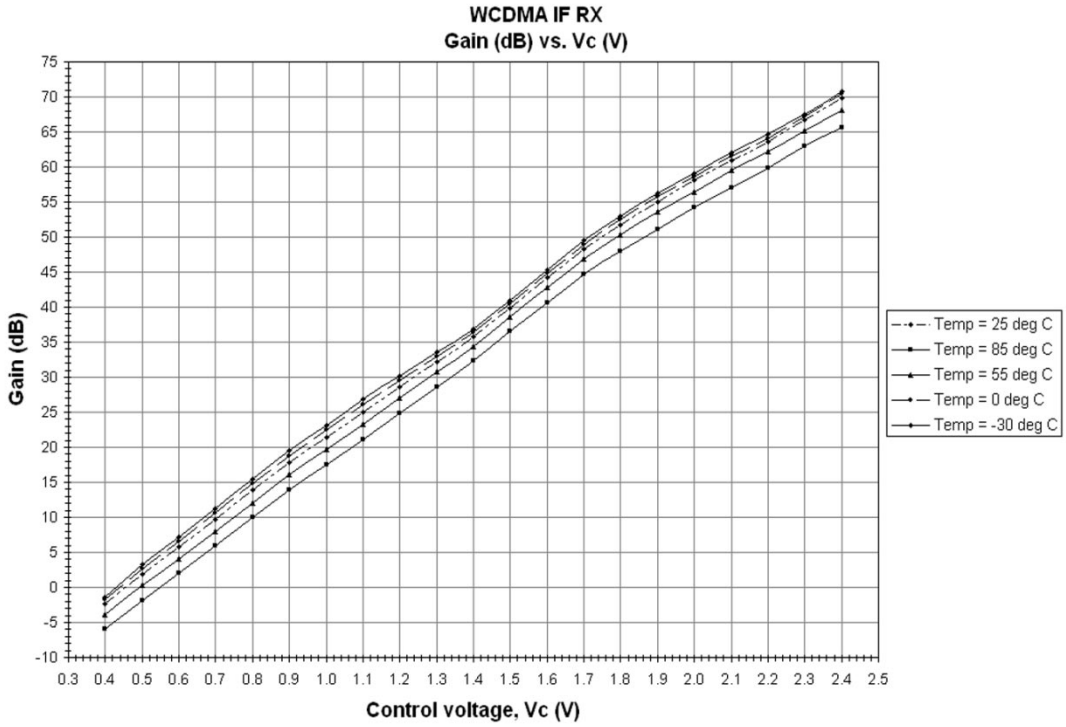

Fig. 5. Gain control characteristics of the receive chip.

be expressed in terms of a simple mathematical relationship. Therefore, the above method is likely to provide a better linearity of the gain control characteristic compared to [7]–[10].

E. Gain Compensating Bias Generator

The FG stages that are responsible for most of the gain need to be compensated against process and temperature variations since no overall negative feedback is used [2], [7]. Fig. 3 also shows the detailed circuitry of the gain compensating bias generator that uses a differential amplifier stage similar to the FG ones. The transistors M_1 and M_2 are of the same type as the differential pair transistors in the FG stages. A small dc voltage appearing across $R_{\rm REF}$ is applied to the inputs of this differential amplifier and a high-gain negative feedback from its outputs is used to adjust its tail current. It can be shown that if the above feedback loop operates properly then

$$(g_m)_{1,2} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_4} \frac{1}{R_{\rm REF}}. \tag{3}$$

It is easy to see now if a current I_B proportional to the tail current of M_1, M_2 is used to bias the FG stages, then the voltage gain of these stages will be given by

$$A_v = g_m R_D = K\left[\frac{R_D}{R_{\rm REF}}\right] \tag{4}$$

where K is a constant and R_D is the parallel combination of the drain resistance of the FG stages and the gate-bias resistor of the next stage. Provided all the resistors are of the same type, it is possible, to a first degree, to ensure that the voltage gains of the FG stages will be independent of process and temperature variations. In fact, all other amplifiers using resistive loads in the chip are biased with I_B to achieve the same benefits. The advantage of this configuration is that a relatively better match can be maintained between the signal amplifiers and the replica amplifier in the master bias circuit.

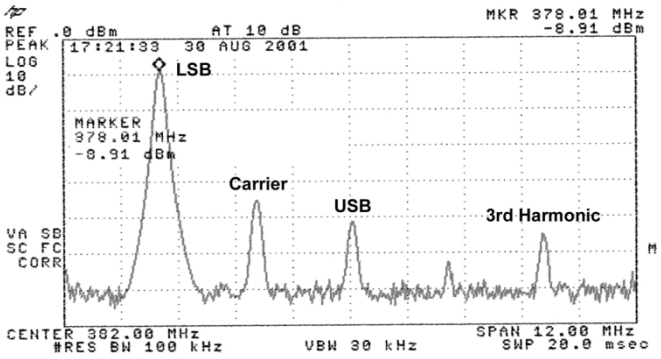

Fig. 6. Output spectrum of the transmit chip with single-component baseband signal.

F. Modulator and Demodulator

The modulator and demodulator designs are also based on Gilbert cell topology [2]. The channel lengths and the layouts of the differential devices and load resistors are carefully optimized to reduce mismatches causing imbalances in the circuits. The circuits are also biased using current from the gain compensating bias generator to stabilize their gains against process and

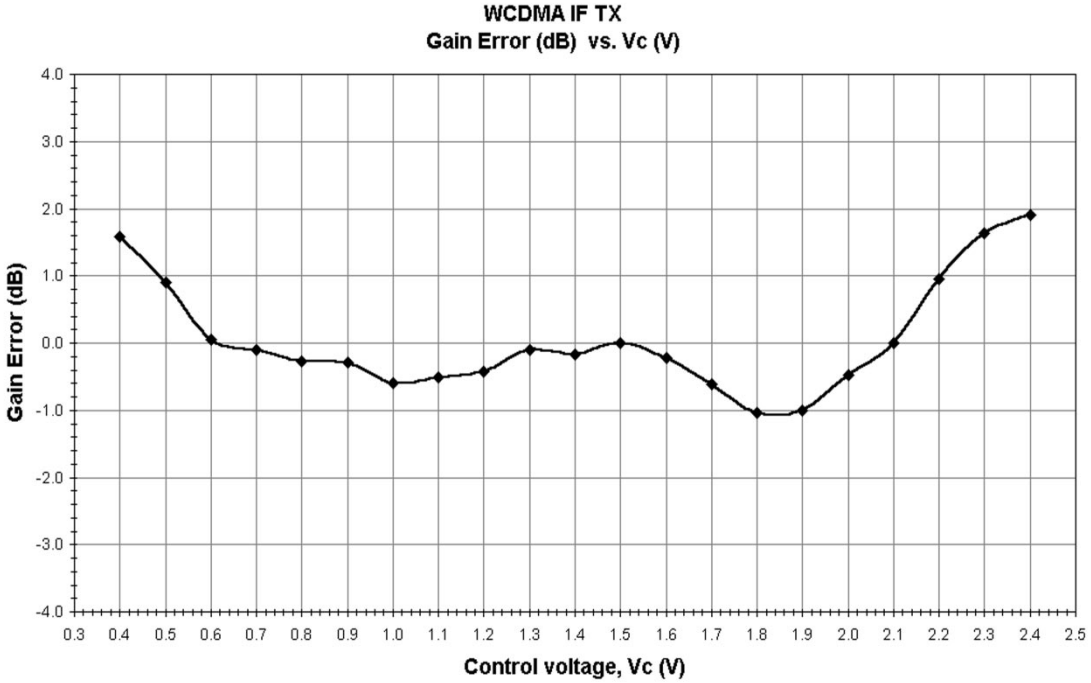

Fig. 7. Linearity error of gain control characteristic for transmit chip.

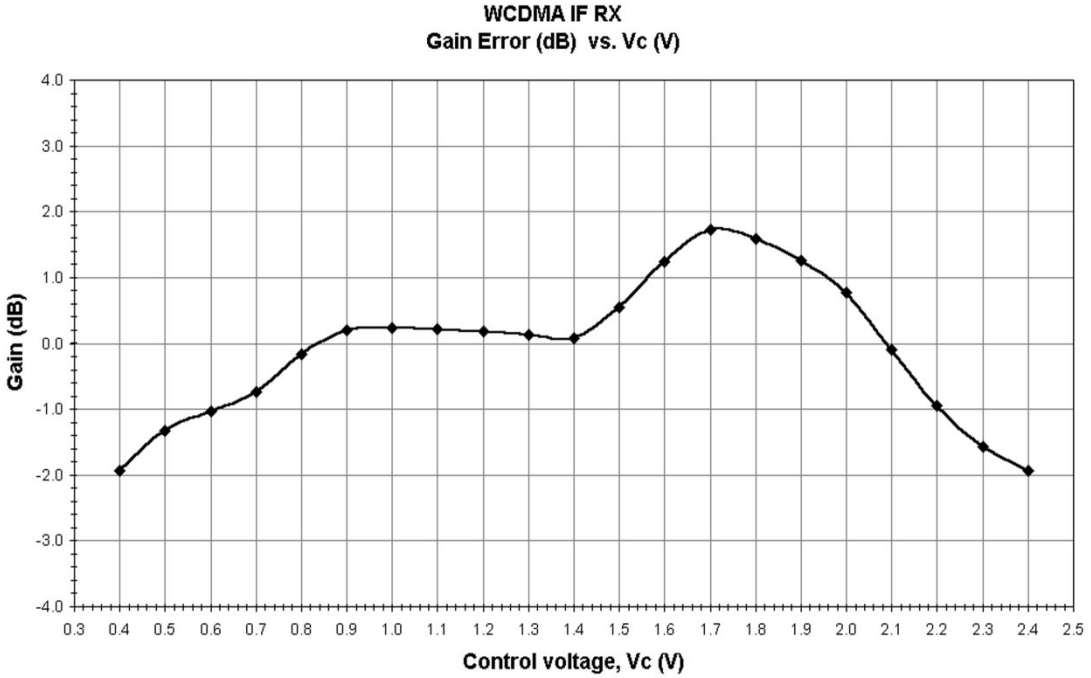

Fig. 8. Linearity error of gain control characteristic for receive chip.

temperature variations. The LO phase shifter uses source-coupled logic (SCL) flip-flops to generate quadrature LO signals by halving the input frequency [5], [11]. The low-frequency baseband output of the demodulator needs to have very small dc offset for direct coupling to the following stage. The dc offset of the LO amplifier also needs to be small for proper operation of the flip-flops. A new technique is employed to overcome this problem and is described below.

If the input transistors of a differential amplifier are of minimum channel length, the tail current splits unequally between the transistors even when the gates at the same potential. This is mainly because of the relatively large mismatch in the channel

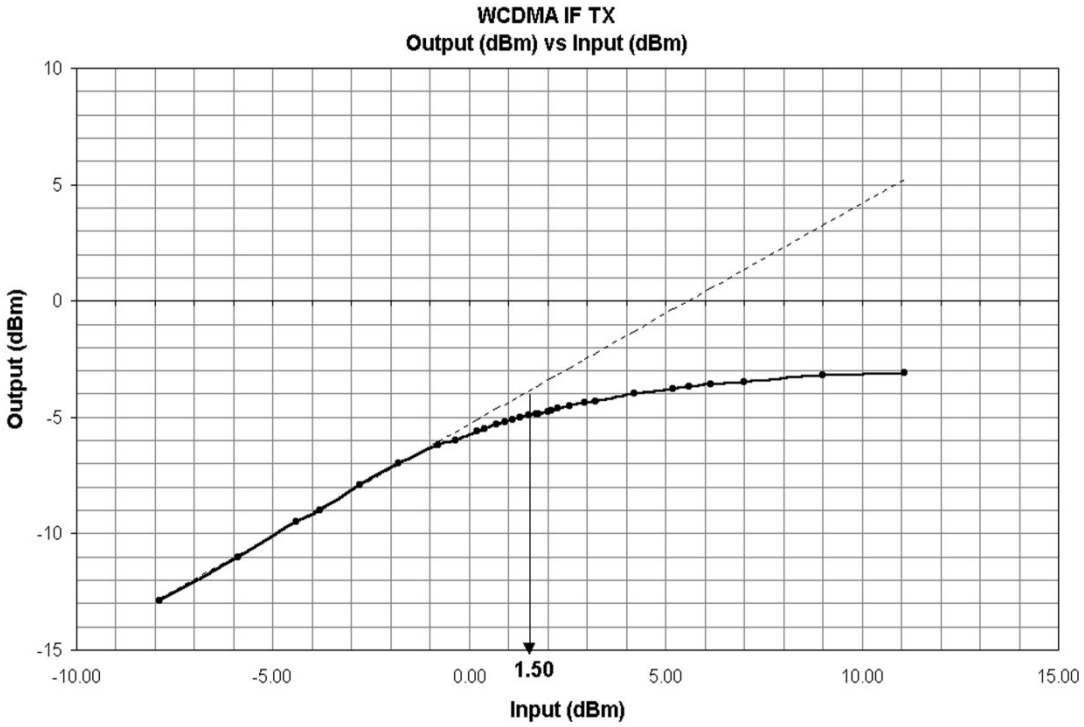

Fig. 9. Input $P1$ dB at maximum gain for transmit chip.

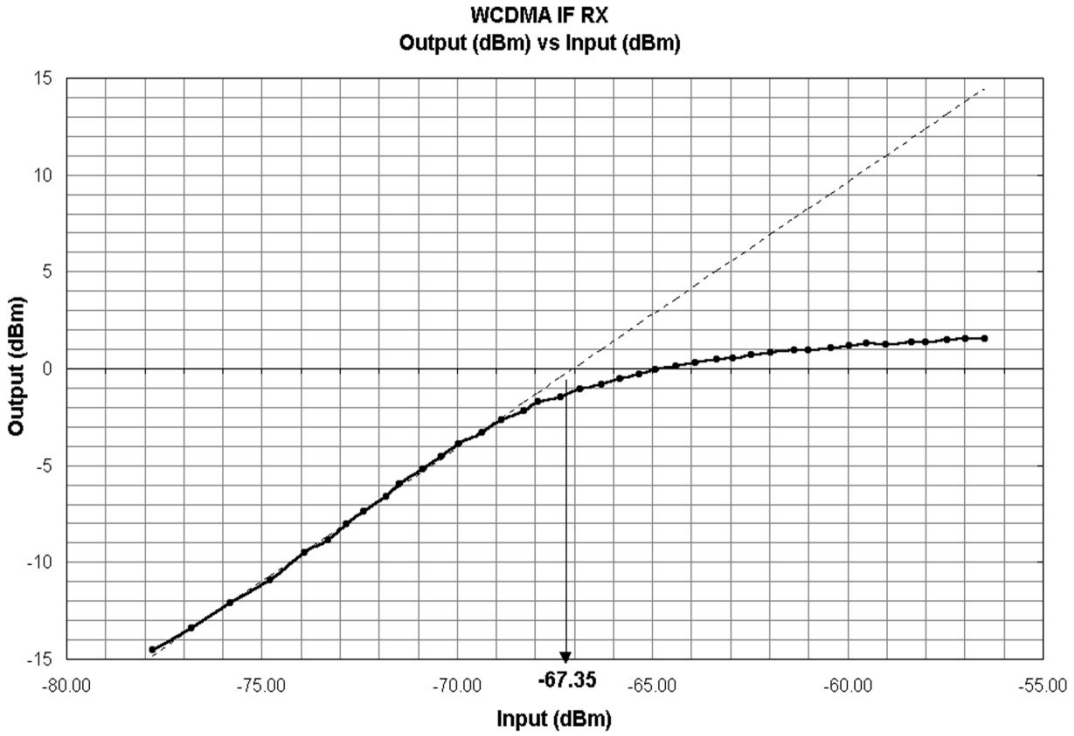

Fig. 10. Input $P1$ dB at maximum gain for receive chip.

length of the devices due to inaccuracies in the poly-gate etching process. The mismatch in channel length results in mismatch in threshold voltage and, consequently, mismatch in the drain currents. Obviously, as discussed earlier, this behavior is totally undesirable for differential operation. Fig. 4 shows how capacitively source-coupled differential stages have been used to minimize the above-mentioned problems in the LO amplifier and the demodulator circuits. With the capacitors C_S, C_S introduced between the source terminals supplied by separate, but identical current sources, the dc current in the differential devices can be identical. The matching of the currents can be arbitrarily improved by implementing the current sources with long

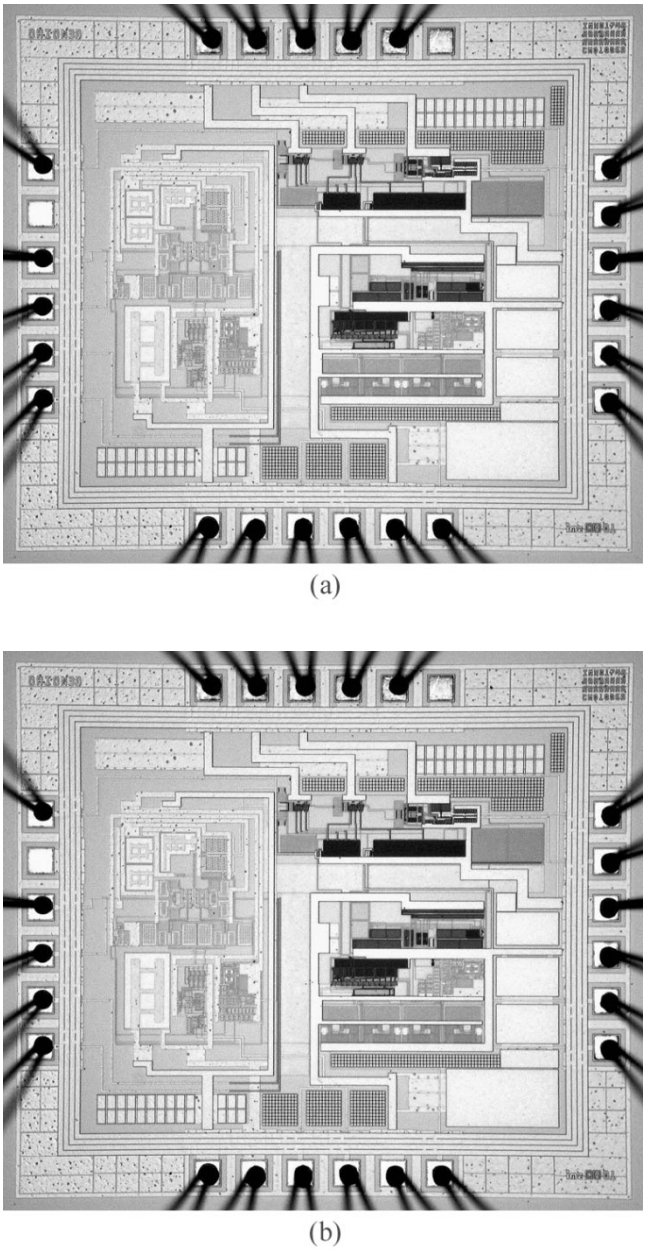

Fig. 11. Chip-set microphotograph. (a) Transmit chip. (b) Receive chip.

channel length devices, as they do not appear in the signal path. At signal frequencies, the impedance of the capacitors are small, and proper differential operation is possible as the connection of the sources is restored. This ensures rail-to-rail LO signals with close to 50% duty cycles to be obtained at the outputs of the LO amplifier. It can also be observed that the output dc offset of the demodulator stage is very low, even if minimum-channel-length differential transistors are used, thus allowing dc coupling of the low-frequency baseband signal to the following stage.

III. Measurement Results

The chip set was fabricated in a standard 0.35-μm two-poly three-metal CMOS process, packaged in a pair of 24-pin ceramic quad flat pack (QFP) packages and mounted on separate double-sided FR4 printed circuit boards (PCBs) for testing.

A summary of the measurement results is shown in Table I. The transmit-chip gain was measured to be from -5 to -73 dB for V_C ranging from 0.4 to 2.4 V. The corresponding figures for the receive chip were from $+70$ to -3 dB. The deviation of the receive gain control characteristic for the specified temperature range was from $+1$ to -4 dB, as shown in Fig. 5. The transmit gain control characteristic also shows a similar deviation.

For the transmit chip, the measured LO, sideband, and third harmonic suppression was -38, -44, and -48 dBc, respectively, as shown in Fig. 6. The adjacent channel power ratio (ACPR) at an average output power level of -10 dBm and the output noise floor for the same chip was measured to be -51 dBc and -123 dBm/Hz, respectively. All the above measurements on the transmit chip was done at maximum gain.

The output I/Q amplitude and phase mismatches for the receive chip were measured to be less than 1.0 dB and $\pm 2^{\circ}$, respectively. The noise figure for the same chip was measured to be 6.4 dB for a source resistance of 1 KΩ at maximum gain.

Figs. 7 and 8 show the deviation of the overall gain control characteristics of the transmit and receive chips from their ideal linear-in-decibel characteristics, respectively. It can be seen from the plots that the deviation measured is within ± 2.0 dB in both cases. The input $P1$ dB (at maximum gain) measurement for the transmit chip is 1.5 dBm and the corresponding figure for the receive chip is -67.35 dBm. These results are shown in Figs. 9 and 10, respectively.

The microphotograph of the chip set is shown in Fig. 11. The measured supply current for the transmit and receive chips were 31 and 17 mA, respectively, with a standby current not exceeding 10 μA for each. On the whole, the measurement results show that the new techniques have been successfully applied.

IV. Conclusion

A 0.35-μm CMOS implementation of the IF sections for WCDMA transceivers in a two-chip set has been presented. Stringent specifications have been met by using minimum-channel-length NMOS devices in frequency critical parts of the circuits. Special circuit techniques have been applied to overcome the associated problems of mismatch, linearity, temperature, and process variations for such short-channel devices. Measurement results in support of such claims have been provided. With more innovative techniques, it might also be possible to integrate the RF sections in CMOS technology in the future.

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